Circuit Scale Minimization Method for Automatic Wiring Diagram Creation of Relay Interlocking Devices

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In automatic generation of wiring diagrams for relay interlocking devices, we have developed a method for minimizing circuit size and a method for minimizing circuit modifications during station modifications. To minimize the circuit size, the equivalent circuit of Boolean algebra is applied to reduce the number of contacts. Then, the wiring diagrams are structured hierarchically so that the equivalent circuit can be applied at each level to deal with complex circuits. Regarding the minimization of circuit changes, we created a circuit in which the contacts before and after the construction were mixed by associating the circuits before and after the construction. Using the created circuit, we made it possible to minimize the changes by the newly devised equivalent circuit before and after the construction.